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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,930	01/29/2004	Shigetaka Kasuga	60188-761	1865

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Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER	
CUTLER, ALBERT H	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/765,930	KASUGA, SHIGETAKA	
	Examiner	Art Unit	
	ALBERT H. CUTLER	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8 and 10-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10,12,13 and 15* is/are allowed.

6)☒ Claim(s) *1 and 16* is/are rejected.

7)☒ Claim(s) *2-6,8,11 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to communication filed on April 1, 2008. Claims 1-6, 8 and 10-16 are pending in the application and have been examined by the Examiner.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 1, 2008 has been entered.

Response to Arguments

3. Applicant's arguments, see pages 2-4, filed April 1, 2008, with respect to the rejection(s) of claim(s) 1 and 16 under 35 U.S.C. 112, 35 U.S.C. 102(b) and 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Goetting et al. (US 5,367,207).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (US 6,115,066) in view of Goetting et al. (US 5,367,207).

Consider claim 1, Gowda et al. teaches:

A solid state imaging device (figures 3 and 4) using N-type MOS transistors as transistors included therein (Column 5, lines 12-13, figure 4), comprising:

a pixel unit (image sensor, 20, figure 3) composed of a plurality of pixels (30) arranged in a two-dimensional matrix (see figure 3), each of said pixels (30) including a photoelectric converting element (26, figure 4) for generating charge in response to light (26 is a photodiode, column 4, lines 23-25.) and an amplifying element (23, figure 4) for outputting, as an analog signal, a voltage signal corresponding to said charge generated by said photoelectric converting element (FET 23 provides a signal directly related to (i.e. an amplified signal) the charge on the photodiode, column 6, lines 19-22.);

a selection signal line (15, figure 3) provided correspondingly to each pixel row (see figure 3) of said pixel unit (20);

a comparison/storage unit (40 and 42, figure 3) provided correspondingly to each pixel column (see figure 3) of said pixel unit (20) for converting, into a digital signal, said analog signal output from said amplifying element (23) included in each pixel (30) belonging to a pixel row selected in said pixel unit (30, see figure 3) and for storing said digital signal (Each pixel row contains an ADC (40) for converting the analog signal into a digital signal, column 6, lines 22-26. This digital signal is then stored in a register (42), column 6, lines 24-26.);

a scanner (44, figure 3) for selecting and reading said digital signal stored in said comparison/storage unit in time series (column 6, line 28 through column 7, line 20); and

an amplifier (44, figure 3) for amplifying said read digital signal and outputting said amplified digital signal to the outside (The "logic block" (44) acts as a differential amplifier by subtracting the reset signals from the data output from the comparison/storage unit, column 3, line 64 through column 4, line 1. Data is output from logic block (44) to image storage and processing electronics (i.e. the outside), column 7, lines 17-21.).

Gowda et al. teaches that the individual photodiodes (30) are comprised of N-type MOS transistors alone ("NMOSFETS", column 5, lines 12-13, figure 5). However, Gowda et al. does not explicitly teach that the entire solid state imaging device is comprised of N-type MOS transistors alone.

Goetting et al. similarly teaches of an integrated circuit array (see title). However, in addition to the teachings of Gowda et al., Goetting et al. teaches the

benefits of using NMOS transistors alone in an integrated circuit (see column 6, lines 2-12). Goetting et al. teaches that these benefits include, among other things, making it possible to save space by packing transistors more closely due to the transistors having the same conductivity type, and simplifying the manufacturing process.

Even if Goetting et al. is not within the same field of endeavor, the Examiner finds that the reference is reasonably pertinent to the problem with which the applicant was involved, namely, using only NMOS transistors in place of circuitry using both NMOS and PMOS transistors, and would have commended themselves to anyone addressing such a problem. See In re Clay, 966 F.2d 656, 658, USPQ2d 1058, 1060 (Fed. Cir. 1992).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to use N-type MOS transistors alone as taught by Goetting et al. in the solid state imaging element taught by Gowda et al. for the benefit of making it possible to save space by packing transistors more closely due to the transistors having the same conductivity type, and simplifying the manufacturing process.

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (US 6,115,066) in view of Goetting et al. (US 5,367,207), as applied to claim 1 above, and further in view of Kim (US 6,423,957).

Consider claim 16, and as applied to claim 1 above, Gowda et al. teach a comparison/storage unit (see claim 1 rationale). However, the combination of Gowda et

al. and Goetting et al. does not explicitly teach the internal contents of said comparison/storage unit.

Kim is similar to Gowda et al. in that Kim teaches a solid state imaging device (figure 4), comprising a pixel unit ("pixel array", 20) formed on a semiconductor substrate and outputting, as an analog signal, a voltage signal corresponding to light (Column 2, lines 52-57) and a comparison/storage unit (30, figure 4), wherein transistors included in said pixel unit are all N-type MOS transistors (An AD converter (30) comprises a comparator (32), a double buffer (40), and a ramp voltage generator (31), figure 4. The AD converter (30) of figure 4 contains the same parts as the AD converter (30) of figure 1. These parts are detailed in figure 2, where a pixel (200) from the pixel unit is shown, and the comparator (320) and double buffer (400) of the AD converter (30) are also shown. All of these devices similarly contain NMOS transistors alone, see figure 2.).

However, in addition to the teachings of the combination of Gowda et al. and Goetting et al., Kim teaches that the comparison/storage unit (30, figure 4, see figure 2) includes an inverter circuit having a booster circuit (See figure 2, the bottom portion clearly contains inverters and a booster circuit ("PRECHARGE").).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to include an inverter circuit having a booster circuit as taught by Kim in the comparison/storage unit taught by the combination of Gowda et al. and Goetting et al. for the benefit of aiding in the effective removal of unexpected pixel

voltage in order to obtain a more desirable signal indicative of the actual object image (Kim, column 1, lines 52-55).

Allowable Subject Matter

8. Claim 10, 12, 13 and 15 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter:

Consider claim 10, the closest prior art, Kim et al. (6,423,957) teaches of a comparator (32, figure 4, 320, figure 2), and of a booster circuit (see claim 7 rationale). However, Kim et al. does not teach or fairly suggest that the comparator has an inverter circuit containing a booster circuit.

Consider claim 12, the closest prior art, Kim et al. (6,423,957) teaches of a memory (40, 400) and a booster circuit (see claim 7 rationale). Kim et al. further teach that said memory (400) includes a plurality of switches (M5-M8, figure 2). However, Kim et al. does not teach or fairly suggest that said memory includes a capacitor or an output amplifier connected to a booster circuit.

Claim 13 is allowable as being dependant upon an allowable claim 12.

Consider claim 15, the closest prior art, Kim et al. (6,423,957) teaches of a counter generator ("COUNT SIGNAL", figure 4), a pulse generator (31 figure 4), and a booster circuit (see claim 7 rationale). However, Kim et al. does not teach or fairly suggest that the said counter generator includes a plurality of inverter circuits each having a booster circuit.

10. Claims 2-6, 8, 11 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

Consider claim 2, the closet prior art, Gowda et al. (US 6,115,066) teaches a comparison/storage unit (see claim 1 rationale). However, Gowda et al. do not teach or fairly suggest that the comparison circuit is comprised of three inverter circuits including three N-type MOS transistors alone or serially connected, or that the resistance of various transistors is increased or decreased to increase the rise speed or fall speed of the inverters.

Claims 3-6, 8, 11 and 14 are allowable as being dependant upon an allowable claim 2.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALBERT H. CUTLER whose telephone number is (571)270-1460. The examiner can normally be reached on Mon-Thu (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan V Ho can be reached on (571)-272-7365. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan V Ho/
Primary Examiner, Art Unit 2622

AC